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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/802,010	CHUNG ET AL.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8-15,and 17* is/are rejected.

7)☒ Claim(s) *7 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 are pending in the instant application. The amendments submitted 4/10/2007 have been entered with the filing of a Request for Continued Examination on 5/14/2007. Applicant's arguments submitted 4/10/2007 have been carefully and fully considered, but they are not persuasive.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. **Claims 2 and 12** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

4. **Claims 2 and 12** recite the limitation "*The method as claimed in claim 11, wherein the meta-information is written after the data of the logical block is written.*" The Examiner is not aware of a portion of the specification which teaches how the meta-information is written after the data of the logical block is written. Accordingly, one of ordinary skill in the art would not know how to make or use the invention as recited in claims 2 and 12.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claims 1, 3-4, 11, and 13-14** are rejected under 35 U.S.C. 102(b) as being anticipated by Conley (US 2002/0099904).

7. **Claim 1** is taught by Conley as:

a. *A flash memory access apparatus, comprising: a flash memory comprising a plurality of units, each of the units comprising a plurality of blocks, and a flash memory controller.* Paragraph 0038 teaches the architecture of a typical non-volatile data storage system, which includes a controller and a plurality of flash memory devices. Paragraph 0040 explains that flash memory cells are divided into multiple pages.

b. *Wherein if a write operation is requested for a logical block number of the flash memory, the flash memory controller is configured to write data and meta-information in a physical block corresponding to a logical block with the logical block number if a previous write operation has not been performed for the logical block.* Paragraph 0062 discusses a method of programming a non-volatile

memory. If there are pages in the physical block that have not been written to, the data is written to those blocks.

c. *And the flash memory controller is configured to perform a write operation for writing the data and the meta-information allocated to the logical block in a new physical block without changing flash memory state information written in a previous physical block corresponding to the logical block if the previous write operation has been performed for the logical block.* Paragraph 0049 shows that when new data is to be written to a logical block corresponding to physical block PBN 0, item 35 of figure 8, which is full, a new physical block PBN 1, item 39 of figure 8, is selected and the new pages are written to PBN 1. Paragraph 0055 shows that an individual page contains data, item 45 of figure 10, and meta-information, item 49 of figure 10. Paragraph 0048 shows that when new pages are written to a logical block, the pages containing the original data are not tagged. The last sentence of paragraph 0047 further emphasizes this by stating "*the writing of the old/new or other flags, as described with respect to FIGS. 6, 7A and 7B, cannot be tolerated.*"

d. *And wherein the flash memory state information is time independent.* Paragraph 0051 shows that the output of a modulo-N counter can be used to generate the value of field 43, which is shown in paragraph 0052 to be used to determine if a block is the most recent block.

8. **Claim 3** is taught by Conley as:

e. *The apparatus as claimed in claim 1, wherein the data and meta-information of the logical block are simultaneously written.* Paragraph 0055 shows that the data 45 and meta-information 49 are part of the same page. As the data and meta-information are part of the same page they would inherently be written simultaneously, as the system of Conley writes data on a page basis.

9. **Claim 4** is taught by Conley as:

f. *The apparatus as claimed in claim 1, wherein the meta-information comprises the logical block number.* Paragraph 0055 shows that overhead data, item 49 of figure 10, contains the logical block number.

g. *And the flash memory state information indicating a state of the physical block as valid, deleted, or invalid.* Paragraph 0055 shows a page contains a time stamp 43, paragraph 0051 shows that the timestamp can be replaced with the output of a modulo-N counter. Paragraph 0050 shows that the time stamp indicates the time the page was written relative to other pages with the same logical address. As shown in paragraph 0052, the time stamps of blocks having the same logical block address and page offset are compared, which allows the system to determine which page is the last written page. Accordingly, this shows what pages are valid.

10. **Claim 11** is taught by Conley as:

h. *A flash memory access method, comprising: accessing the flash memory and searching for a currently writable physical block if a processor requests a write operation for a specific logical block number of the flash memory.* Paragraph 0062 shows that when a write is performed, an available physical page is found.

i. *And writing data and meta-information in a physical block corresponding to a logical block with the logical block number if a previous write operation has not been performed for the logical block.* Paragraph 0062 discusses a method of programming a non-volatile memory. If there are pages in the physical block that have not been written to, the data is written to those blocks.

j. *And writing the data and the meta-information in a new physical block corresponding to the logical block without changing flash memory state information written in a previous physical block corresponding to the logical block the previous write operation has been performed for the logical block.* Paragraph 0049 shows that when new data is to be written to a logical block corresponding to physical block PBN 0, item 35 of figure 8, which is full, a new physical block PBN 1, item 39 of figure 8, is selected and the new pages are written to PBN 1. Paragraph 0055 shows that an individual page contains data, item 45 of figure 10, and meta-information, item 49 of figure 10. Paragraph 0048 shows that when new pages are written to a logical block, the pages containing the original data are not tagged. The last sentence of paragraph 0047 further emphasizes this by

stating "*the writing of the old/new or other flags, as described with respect to FIGS. 6, 7A and 7B, cannot be tolerated.*"

k. *Wherein the flash memory state information is time independent.* Paragraph 0051 shows that the output of a modulo-N counter can be used to generate the value of field 43, which is shown in paragraph 0052 to be used to determine if a block is the most recent block.

11. **Claim 13** is taught by Conley as:

l. *The apparatus as claimed in claim 11, wherein the data and meta-information of the logical block are simultaneously written.* Paragraph 0055 shows that the data 45 and meta-information 49 are part of the same page. As the data and meta-information are part of the same page they would inherently be written simultaneously, as the system of Conley writes data on a page basis.

12. **Claim 14** is taught by Conley as:

m. *The method as claimed in claim 11, wherein the meta-information comprises the logical block number.* Paragraph 0055 shows that overhead data, item 49 of figure 10, contains the logical block number.

n. *And the flash memory state information indicating a state of the physical block as valid, deleted, or invalid.* Paragraph 0055 shows a page contains a time stamp, paragraph 0051 shows that the timestamp can be replaced with the output of a modulo-N counter. Paragraph 0050 shows that the time stamp

indicates the time the page was written relative to other pages with the same logical address. As shown in paragraph 0052, the time stamps of blocks having the same logical block address and page offset are compared, which allows the system to determine which page is the last written page. Accordingly, this shows what pages are valid.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. **Claims 5-6, 8-10, 15, and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Conley (cited *supra*) in view of Kim et al. (US 6,381, 176).

15. **Claim 5** is taught by Conley as shown *supra* with respect to claim 1.

16. Although Conley teaches that blocks having the same logical block number can be distinguished by their timestamps, it does not disclose expressly performing a recovery operation.

17. With respect to claim 5, Kim teaches:

o. *The apparatus as claimed in claim 1, wherein the flash memory controller is configured to perform a recovery operation which detects, during a scanning*

process, physical blocks for the logical block number and recovers from an error by determining a valid block for the logical block among the detected physical blocks. Kim teaches at column 6 lines 29-36 that a recovery operation is required if two valid blocks having the same logical block number exist. In the system disclosed by Conley, paragraph 0050 shows that it can be determined which of multiple pages having the same logical block number and page offset is the correct page by comparing the timestamps of the blocks.

18. At the time of the invention it would have been obvious to one of ordinary skill in the art that a recovery operation is necessary in the event of an error during writing.

19. Conley and Kim are analogous art because they are from the same field of endeavor, the design of flash memory systems.

20. The motivation for doing so would have been to determine which block will be erased during a recovery operation (Kim, column 6 lines 30-36)

21. Therefore, it would have been obvious to combine Kim with Conley for the benefit of determining which pages are old and can be deleted to obtain the invention as specified in **claims 5, 6, and 8-10**.

22. **Claim 6** is taught by Conley as:

p. *The apparatus as claimed in claim 5, wherein the scanning process comprises reading a logical block number for each of the physical blocks by investigating the flash memory based on a latest accessed block.* Paragraph

0052 shows that when the controller reads the data, it compares the counts in fields 43 and 43' of pages having the same LBA and page offset.

q. *And investigating a field of a block allocation table corresponding to the read logical block number.* Figure 9, discussed in paragraph 0049, which is formed from the data in fields 41 and 41', shows the table that provides a mapping from logical blocks to physical blocks.

23. **Claim 8** is taught by Conley as:

r. *The apparatus as claimed in claim 5, wherein the recovery operation recovers from an error by determining a latest accessed physical block for the logical block number among the detected physical blocks according to priorities set during the scanning process, as the valid block.* Conley paragraph 0050 shows that the most recently written page is determined by checking field 43, the timestamp.

s. *And rewriting flash memory state information written in other physical blocks of the detected physical blocks as deleted.* Paragraph 0062 shows that updating one or more blocks of data will result in one or more blocks storing the data to be superceded by the new data, and the blocks with superceded data are identified for erasure.

24. **Claim 9** is taught by Conley and Kim as:

t. *The apparatus as claimed in claim 5, wherein the recovery operation is performed during the initializing the flash memory.* Kim column 4 lines 22-25 shows that when a flash memory is initially used, a logical unit number to physical unit number table is provided. To generate such a table in a system using the timestamps of Conley, it would be necessary to determine which of the pages sharing the same logical block number and page offset is the most recent page.

25. **Claim 10** is taught by Kim as:

u. *The apparatus as claimed in claim 5, wherein the recovering from the error is performed during reclaiming the flash memory wherein the reclaiming comprises moving data written in a predetermined unit of the flash memory to a new unit.* Column 8 line 55 to column 9 line 4 teaches that in a reclaim operation, valid blocks and related metadata are copied to a new unit. In order to determine which blocks are valid in a system using the timestamps of Conley, the timestamps of pages having the same logical block number and page offset must be compared.

26. **Claim 15** is taught by Conley as shown *supra* with respect to claim 11.

27. Although Conley teaches that blocks having the same logical block number can be distinguished by their timestamps, it does not disclose expressly performing a recovery operation.

28. With respect to claim 5, Kim teaches:

v. *The method as claimed in claim 11, further comprising a recovery operation comprising detecting, during a scanning process, physical blocks for the logical block number and of recovering from an error by determining a valid block for the logical block among the detected physical blocks.* Kim teaches at column 6 lines 29-36 that a recovery operation is required if two valid blocks having the same logical block number exist. In the system disclosed by Conley, paragraph 0050 shows that it can be determined which of multiple pages having the same logical block number and page offset is the correct page by comparing the timestamps of the blocks.

29. At the time of the invention it would have been obvious to one of ordinary skill in the art that a recovery operation is necessary in the event of an error during writing.

30. Conley and Kim are analogous art because they are from the same field of endeavor, the design of flash memory systems.

31. The motivation for doing so would have been to determine which block will be erased during a recovery operation (Kim, column 6 lines 30-36)

32. Therefore, it would have been obvious to combine Kim with Conley for the benefit of determining which pages are old and can be deleted to obtain the invention as specified in **claims 15 and 17**.

33. **Claim 17** is taught by Conley and Kim as:

w. *The method as claimed in claim 15, wherein the recovering comprises recovering from the error by determining a latest data written among data of a specific logical block number detected during reclaiming the flash memory and wherein the reclaiming comprises moving data written in a predetermined unit of the flash memory to a new unit.* Conley paragraph 0050 shows that the most recently written page is determined by checking field 43, the timestamp. Kim column 8 line 55 to column 9 line 4 teaches that in a reclaim operation, valid blocks and related metadata are copied to a new unit. In order to determine which blocks are valid in a system using the timestamps of Conley, the timestamps of pages having the same logical block number and page offset must be compared.

Response to Arguments

34. Applicant's arguments submitted 4/10/2007 have been carefully and fully considered, but are not persuasive.

35. **First point of Argument**

36. Applicant's arguments with respect to the rejection of claims 2 and 12 under 35 USC 112 second paragraph, see the second paragraph on page 7 through the second paragraph beginning on page 8, have been carefully and fully considered, but are not persuasive. Applicant argues "*In other words, the data and meta-information can be written simultaneously if the atomicity for a write operation on a block basis is ensured. However, as indicated by the above-cited portion of the specification, atomicity of the*

blocks is not required. The data and meta-data information could, for example, be written at different times if the main area of the block and the spare area of the block are physically separate blocks, each capable of being written to at different times." Although this may be true, it is not taught in the specification that the main area of a block and the spare area of the block are physically separate blocks. Further, this interpretation is inconsistent with the language of the claims. Claim 1 recites "*the flash memory controller is configured to write data and meta-information in* ***a physical block***" (emphasis added). Stating that one of ordinary skill in the art could write the data and meta-information in physically separate blocks does not provide enablement for writing meta-information after the data of the logical block is written when the meta-information and data are required to be written in a physical block. As described in paragraph 05 of the specification as originally filed, the block is the unit of data that can be read or written in a read or write operation.

37. **Second point of Argument**

38. Applicant's arguments with respect to the rejection of claims 1, 3, 4, 11, 13, and 14 under 35 USC 102(b) as being anticipated by Conley, see the fourth paragraph beginning on page 8 through the final paragraph beginning on page 9, have been carefully and fully considered, but are not found persuasive. Applicant argues "*furthermore, claim 1 does not write merely recite writing the data and the meta-information without changing state information. On the contrary, claim 1 recites writing the data and the metadata-information allocated to the logical block in a new physical block without changing flash memory state information written in a previous physical*

block." The examiner respectfully disagrees with Applicant's conclusion. Claim 1 does not recite a step in which flash memory information is written to a block. Claim 1 does not recite that any physical block contains flash memory state information. Claim 1 recites "*the flash memory is configured to perform a write operation for writing the data and the meta-information allocated to the logical block in a new physical block without changing flash memory state information written in a previous physical block corresponding to the logical block if the previous write operation has been performed for the logical block*". This limitation, given broadest reasonable interpretation, requires that flash memory state information written in a previous physical block is not changed. If there is no flash memory state information written in a previous block, there is no flash memory state information to change, and therefore it is not possible for the controller to change flash memory state information written in the previous physical block. Accordingly, if there is no flash memory state information written in a previous block of Conley, there is no flash memory state information to change, and therefore, the system of Conley would write the data and meta-information in a new physical block without changing flash memory state information written in a previous physical block.

39. Applicant is encouraged to amend independent claims 1 and 11 to positively recite that written blocks contain flash memory state information, to clarify that the claims require flash memory state information, if that is the intended scope of the claims.

40. **Third point of Argument**

41. Applicant's arguments with respect to the rejection of claims 1, 3, 4, 11, 13, and 14 under 35 USC 102(b) as being anticipated by Conley, see the first paragraph beginning on page 10 through the second paragraph beginning on page 11, have been carefully and fully considered, but are not persuasive. Paragraph 0051 of Conley teaches that the output of a modulo-N counter may be used in field 43 instead of a timestamp.

42. **Fourth point of Argument**

43. Applicant's arguments with respect to the rejection of claims 5 and 15 under 35 USC 103(a) as being unpatentable over Conley in view of Kim, see the third paragraph beginning on page 11 through the final paragraph beginning on page 12, have been carefully and fully considered, but are not found persuasive. Applicant argues "*it would be unnecessary, and inefficient to the operation of Conley, to perform an extra block recovery operation as disclosed in Kim. Indeed, any such modification of Conley, as the Examiner contends, would impermissibly destroy the principle operation of Conley.*" The Examiner respectfully disagrees. The Examiner does not rely on Kim to teach a recovery method, Kim is merely relied upon to show that a recovery operation is required if two valid blocks have the same logical number. As stated in the Office action with respect to claims 5 and 15, the mechanisms of Conley are sufficient to perform the recovery operation. As argued by applicant in the first paragraph beginning on page 12, the timestamp/modulo-N counter of Conley provide sufficient mechanisms to perform the recovery operation, therefore, Kim was not relied upon for this teaching. However, as Conley does not expressly recite performing the recited recovery operation, Kim was

relied upon to show that it would be obvious to one of ordinary skill in the art to perform such an operation.

Allowable Subject Matter

44. **Claims 7 and 16** are objected to as being dependent upon a rejected base claim, but may be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

45. **Claim 7** recites the limitation "*wherein the investigating the field of the block allocation table comprises writing a state value of "1" in the field of the block allocation table if the state value has been "0" and detecting that the logical block number has been searched for through the previous physical block during the scanning process, if the state value is "1".*" This limitation in combination with the other recited limitations is not taught or suggested by the prior art of record.

46. **Claim 16** recites the limitation "*And writing a state value of "1" in the field of the block allocation table if the state value has been "0" and detecting that the logical block number has been searched for through the previous physical block during the scanning process, if the state value is "1".*" This limitation in combination with the other recited limitations is not taught or suggested by the prior art of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jared I Rutz
Examiner
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jir

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